CLAIMS

1. (original) A method for forming a semiconductor device comprising:
   providing a semiconductor substrate;
   forming an insulating layer on a surface of the semiconductor substrate;
   providing a strained semiconductor layer on the insulating layer;
   defining a <100> direction of the strained semiconductor layer; and
   forming a transistor on the strained semiconductor layer, wherein the transistor is aligned along the <100> direction of the strained semiconductor layer.

2. (original) The method of claim 1, wherein the strained semiconductor layer is in a tensile stress state.

3. (original) The method of claim 1, wherein providing a strained semiconductor layer further comprises:
   providing an at least partially relaxed silicon-germanium layer on the insulating layer; and
   forming a silicon layer on the at least partially relaxed silicon-germanium layer to form the strained semiconductor layer.

4. (original) The method of claim 1, wherein providing a strained semiconductor layer on the insulating layer comprises:
   forming a semiconductor layer on the insulating layer; and
   straining the semiconductor layer.

5. (original) The method of claim 1, further comprising defining a <110> direction of the semiconductor substrate.

6. (original) The method of claim 5, further comprising aligning the <110> direction with the <100>.

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7. (original) A method for forming a semiconductor device comprising:

providing a semiconductor substrate;

defining a <110> direction of the semiconductor substrate;

forming an insulating layer on a surface of the semiconductor substrate;

providing a pre-strained semiconductor layer;

defining a <100> direction of the pre-strained semiconductor layer;

bonding the pre-strained semiconductor layer to the insulating layer, wherein the <100> of the pre-strained semiconductor layer is aligned with the <110> direction of the semiconductor substrate; and

forming a transistor on the pre-strained semiconductor layer, wherein the transistor is aligned along the <100> direction of the pre-strained semiconductor layer.

8. (original) The method of claim 7, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer.

9. (original) The method of claim 7, wherein the semiconductor device is characterized as being a silicon-on-insulator device.

10. (original) The method of claim 7, wherein bonding of the pre-strained semiconductor layer to the insulating layer is performed by thermal wafer bonding.

11. (original) The method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

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12. (original) The method of claim 7, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

13. (original) The method of claim 7, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

14. (currently amended) ~~The~~ A method ~~of claim 13~~ for forming a semiconductor device, ~~further~~ comprising:

providing a semiconductor substrate;
defining a <110> direction of the semiconductor substrate;
forming an insulating layer on a surface of the semiconductor substrate;
providing a pre-strained semiconductor layer on a SiGe layer;
defining a <100> direction of the pre-strained semiconductor layer;
bonding the pre-strained semiconductor layer to the insulating layer, wherein the <100> of the pre-strained semiconductor layer is aligned with the <110> direction of the semiconductor substrate;
cleaving the SiGe layer to leave a remaining portion of the SiGe layer on the pre-strained semiconductor layer; and
removing the ~~pre-strained semiconductor~~ remaining portion of the SiGe layer after cleaving; and
forming a transistor on the pre-strained semiconductor layer, wherein the transistor is aligned along the <100> direction of the pre-strained semiconductor layer;

15. (original) A method for forming a semiconductor device comprising:

providing a semiconductor substrate;
defining a crystal orientation of the semiconductor substrate;
forming an insulating layer on a surface of the semiconductor substrate;
providing a pre-strained semiconductor layer;
defining a crystal orientation of the pre-strained semiconductor layer;

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bonding the pre-strained semiconductor layer to the insulating layer, wherein the crystal orientation of the pre-strained semiconductor layer is not aligned with the crystal orientation of the semiconductor substrate; and

forming a transistor on the pre-strained semiconductor layer, wherein a source/drain axis of the transistor is aligned along the crystal orientation of the pre-strained semiconductor layer.

16. (original) The method of claim 15, wherein the crystal orientation of the pre-strained semiconductor layer is determined to enhance current transport capability of a PMOS transistor.

17. (original) The method of claim 15, wherein the semiconductor device is a silicon-on-insulator device.

18. (original) The method of claim 15, wherein providing a pre-strained semiconductor layer further comprises:

providing an at least partially relaxed silicon-germanium layer; and

forming a silicon layer on the at least partially relaxed silicon-germanium layer form the pre-strained semiconductor layer.

19. (original) The method of claim 15, wherein defining a crystal orientation of the semiconductor substrate comprises defining a <110> direction of the semiconductor substrate.

20. (original) The method of claim 15, wherein defining a crystal orientation of the pre-strained semiconductor layer comprises defining a <100> direction of the pre-strained semiconductor layer.

21. (original) The method of claim 20, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor along the <100> direction of the pre-strained semiconductor layer.

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22. (original) The method of claim 21, wherein forming a transistor on the pre-strained semiconductor layer comprises aligning a source/drain axis of the transistor perpendicular to the <100> direction of the pre-strained semiconductor layer.

23. (original) The method of claim 15, further comprising cleaving the semiconductor device through the pre-strained semiconductor layer.

24. (original) The method of claim 15, further comprising polishing the pre-strained semiconductor layer after cleaving.

25. (withdrawn) A semiconductor device comprising:

a semiconductor substrate having a first crystal orientation;

an insulating layer formed on a surface of the semiconductor substrate; and

a pre-strained semiconductor layer bonded to the insulating layer, the pre-strained semiconductor layer having transistors formed thereon, wherein channel regions of the transistors are aligned with a second crystal orientation, the second crystal orientation being different than the first crystal orientation.

26. (withdrawn) The semiconductor device of claim 25, wherein the pre-strained semiconductor layer is in a tensile stress state.

27. (withdrawn) The semiconductor device of claim 25, wherein the pre-strained semiconductor layer is formed by depositing a silicon layer on an at least partially relaxed silicon-germanium layer.

28. (withdrawn) The semiconductor device of claim 25, wherein the second crystal orientation is along a natural cleave plane of the pre-strained semiconductor layer, and the first crystal orientation is aligned 45 degrees from the second crystal orientation.

29. (withdrawn) The semiconductor device of claim 25, wherein the second crystal orientation is rotated 45 degrees from the first crystal orientation.

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30. (withdrawn) The semiconductor device of claim 25, wherein the channel regions of the transistors are aligned in a <100> direction.

31. (withdrawn) The semiconductor device of claim 25, wherein the semiconductor device is a silicon-on-insulator device.

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